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(54) Scrambler for Q-mode and data-mode transmission

(57) In a data communication system, a transmitter of a modem, for example, uses a single scrambler to operate in a data communication mode and in a non-data mode. During the data communication mode the scrambler is used to scramble data for communication by the transmitter. During the non-data mode, the scrambler is used to generate a non-data mode signal for communication by the scrambler. The modem may be an ADSL modem, for example, in which case the data communication mode is SHOWTIME while the non-data mode may be Q-mode.

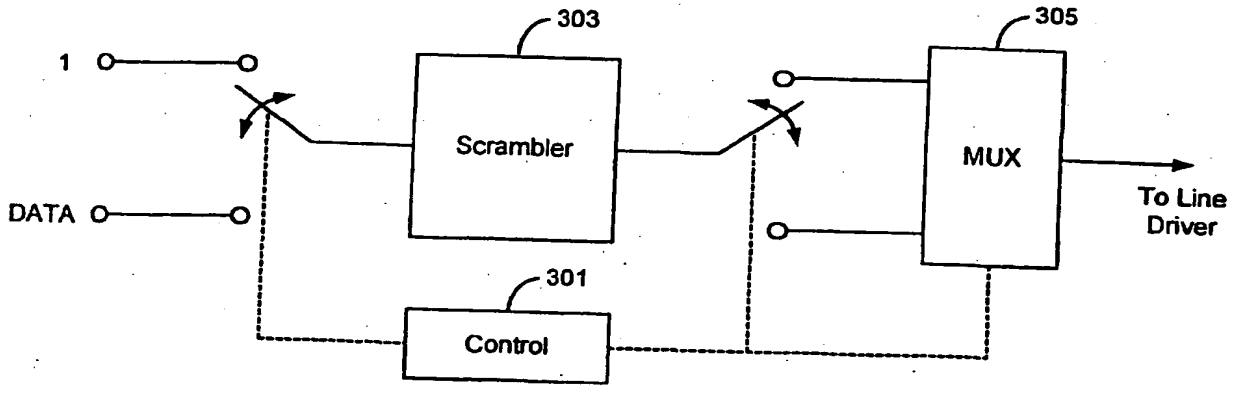

Fig. 3

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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application makes reference to, and claims priority to and the benefit of, United States provisional application Serial No. 60/241,126 filed October 16, 2000.

INCORPORATION BY REFERENCE

[0002] The above-referenced United States provisional application Serial No. 60/241,126 is hereby incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0003] Current ADSL modem system designs do not incorporate a low power transmission mode. Such systems require high power dissipation in the modem line driver, even when no data is being transmitted.

[0004] Accordingly, ITU contributions have proposed a low power mode (i.e., "Q-mode,") in the transmitter. During the proposed Q-mode, the modem is still in the ready state, but enters a low power mode during periods of no data transmission.

[0005] One ITU contribution, HC-029R1, formally defines a semi-stationary Q-mode signal, that employs a pair of pseudo-random bit sequence ("PRBS") generators, each with a period of greater than 4000. One problem with this proposal, however, is that the receiver would require synchronization to two PRBS generators. In addition, requiring two PRBS generators as such correspondingly requires additional hardware in the modem, as well as additional overhead associated with the overall system. Moreover, during the non-Q-mode periods of operation, i.e., during data mode or "SHOWTIME," the two PRBS generators sit idle.

[0006] Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with the present invention as set forth in the remainder of the present application with reference to the drawings.

BRIEF SUMMARY OF THE INVENTION

[0007] Aspects of the present invention may be found in communication system having a data communication node. The data communication node may be, for example, a modem (such as an ADSL modem). The data communication node in turn has a transmitter, which itself has a scrambler.

[0008] The transmitter uses the scrambler to operate in two modes. The first mode is a data communication mode, which, in the case when the data communication node is an ADSL modem, is SHOWTIME. During the data communication mode, the scrambler is used to scramble data that is communicated by the transmitter.

[0009] The second mode is a non-data mode, which in the case when the data communication node is an ADSL transmitter, may be Q-mode. During the non-data mode, the scrambler is used to generate a non-data mode signal.

[0010] In one embodiment of the invention, a determination is made whether data is present at one or more inputs to the system. If it is determined that data is present, a determination is then made whether the scrambler is configured for the data communication mode. If it isn't, the scrambler is configured for the data communication mode, and the system operates in that mode. If it is indeed configured for the data communication mode, then the system simply operates in that mode.

[0011] If it is determined that no data is present, a determination is then made whether the scrambler is configured for the non-data mode. If it isn't, the scrambler is configured for the non-data mode, and the system operates in that mode. If it is indeed configured for the non-data mode, then the system simply operates in that mode.

[0012] In one embodiment of non-data mode operation, a non-data mode input to the scrambler is selected. A non-data mode signal is then generated, using a first output of the scrambler. Next, the non-data mode signal is output, using a second output of the scrambler, for communication by the transmitter. This process is repeated for successive outputs of the scrambler, for as long as the non-data mode input to the scrambler is selected.

[0013] These and other advantages and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0014] Fig.1 is a block diagram of a generic communication system that may be employed in connection with the present invention.

[0015] Fig. 2 is a functional block diagram of an ADSL modem transmitter according to the present invention.

[0016] Fig. 3 is a schematic block diagram illustrating one embodiment by which the scrambler of Fig. 2 performs the two functions shown in Fig. 2.

[0017] Fig. 4 is a block diagram of one embodiment of Q-mode signal generation circuitry in accordance with the present invention.

[0018] Fig. 5 illustrates a more detailed embodiment of the Q-mode signal generation circuitry of Fig. 4.

[0019] Fig. 6 is a flow diagram of overall control for mode selection in accordance with the present invention.

[0020] Fig. 7 is a depiction of a generic scrambler that may be employed in connection with the present invention.

[0021] Fig. 8 is one specific embodiment of a scrambler that may be employed in connection with the present invention.

[0022] Fig. 9 is a scrambler based on the scrambler of Fig. 8 but with alternate outputs selected in such a way that two separate output streams are produced.

[0023] Fig. 10 is a depiction of a generic PRBS generator in accordance with the present invention.

[0024] Fig. 11 is one specific embodiment of the PRBS generator of Fig. 10 in accordance with the present invention.

[0025] Fig. 12 is a PRBS generator based on the PRBS generator of Figure 11, but with alternate outputs selected in such a way that two separate output streams are produced, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Fig.1 is a block diagram of a generic communication system that may be employed in connection with the present invention. The system comprises a first communication node 101, a second communication node 111, and a channel 109 that communicatively couples the nodes 101 and 111. The communication nodes may be, for example, ADSL modems or any other type of transceiver device that transmits or receives data over a channel. The first communication node 101 comprises a transmitter 105, a receiver 103 and a processor 106. The processor 106 may comprise, for example, a microprocessor. The first communication node 101 is communicatively coupled to a user 100 (e.g., a computer) via communication link 110, and to the channel 109 via communication links 107 and 108.

[0027] Similarly, the second communication node 111 comprises a transmitter 115, a receiver 114 and a processor 118. The processor 118, like processor 106, may comprise, for example, a microprocessor. The second communication node 111 is likewise communicatively coupled to a user 120 (again a computer, for example) via communication link 121, and to the channel 109 via communication links 112 and 113.

[0028] During operation, the user 100 can communicate information to the user 120 using the first communication node 101, the channel 109 and the second communication node 111. Specifically, the user 100 communicates the information to the first communication node 101 via communication link 110. The information is transformed in the transmitter 105 to match the restrictions imposed by the channel 109. The transmitter 105 then communicates the information to the channel 109 via communication link 107. The receiver 114 of the second communication node 111 next receives, via communication link 113, the information from the channel 109 and transforms it into a form usable by the user 120. Finally, the information is communicated from the second communication node 111 to the user 120 via the communication link 121.

[0029] Communication of information from the user 120 to the user 100 may also be achieved in a similar manner. In either case, the information transmitted/received may also be processed using the processors 106/118.

[0030] Fig. 2 is a functional block diagram of an ADSL modem transmitter according to the present invention. A transmitter 201 comprises a scrambler 203 and control 205. Control 205 causes the transmitter 201 to operate in two different modes, namely a data transmission or "SHOWTIME" mode (designated functionally by block 207) and a non-data mode or "Q-mode" (designated functionally by block 209). The non-data mode may be, for example, a quiescent, low power mode. While a switch 211 is shown in Fig. 2 as selecting between the data and non-data modes, the switch 211 is not necessarily a hardware switch per se, but rather an abstract selection mechanism, as explained more completely below.

[0031] Fig. 3 is a schematic block diagram illustrating one embodiment by which the scrambler of Fig. 2 performs the two functions shown in Fig. 2. Similar to control 205 of Fig. 2, control 301 acts as a selector between Q-mode operation and data operation. In Q-mode, control 301 selects "1" as the input to scrambler 303, employs the scrambler 303 output for Q-mode purposes, and selects the Q-mode signal as the output of multiplexor 305.

[0032] In data mode, control 301 selects the input of scrambler 303 to be unscrambled data, employs the output of the scrambler 303 to be scrambled data, and selects the data mode signal as the output of mutiplexor 305. In either mode, the output of multiplexor 305 is sent to a line driver (not shown).

[0033] As can be appreciated from Figs. 2 and 3, a single scrambler is used to scramble the data during data transmission and to control the generation of the Q-mode signal.

[0034] Fig. 4 is a block diagram of one embodiment of Q-mode signal generation circuitry in accordance with the present invention. When Q-mode is selected (i.e., "1" at the input of scrambler 401), the scrambler 401 switches be-

tween generating the Q-mode signal and outputting the Q-mode signal. More specifically, for each symbol of the Q-mode signal, two successive outputs from the scrambler 401 are used. The first out put selects whether the basic symbols (i.e., S1 and S2) or their inverses should be generated. In the embodiment of Fig. 4, if the first output is "0," then S1 and S2 are presented at the input of multiplexor 403. If instead the first output is "1," then the inverse of S1 and S2 are presented at the inputs of multiplexor 403.

[0035] The second output of scambler 401 is then presented to control 405, which selects the output of the multiplexor 401. The output of multiplexor 410 represents the Q-mode signal.

[0036] Fig. 5 illustrates a more detailed embodiment of the Q-mode signal generation circuitry of Fig. 4. A scrambler 501 with its input clamped to one generates an output sequence of bits at a rate equal to twice the symbol rate of the system. The outputs of the scrambler 501 are alternately connected to a first input 505 and a second input 507 by means of a switch 503. The first input 505 is used by multiplier 513 to either invert or not invert (i.e. multiply by +1 or -1) a stationary signal 509, resulting in a first signal 514. The same first input 505 also is used by multiplier 515 to either invert or not invert a non-stationary signal 511, resulting in a second signal 516. The first signal 514 and the second signal 516 form the inputs to a multiplexor 517.

[0037] The second input 507 is applied to the input of a serial-to-parallel convertor 531 that converts groups of bits from the second input 507 to a first 8-bit integer 535. A duty cycle 533 (i.e. a positive number between 0 and 1) is scaled in scaler 534 to an 8-bit positive integer (i.e., an integer between 0 and 255 inclusive) to produce a second 8-bit integer 537. A comparator 539 produces an output 518 that is 1 whenever the first 8-bit integer 535 is less than the second 8-bit integer 537; the output 518 is 0 otherwise. The output 518 is the select input 519 of multiplexor 517. The output of multiplexor 517 is Q-mode signal 521, which is comprised of first signal 514 whenever the select input 519 is "1," and second signal 516 whenever the select input 519 is "0."

[0038] A final multiplexor 525, operating under control of Q-mode enable 527, has an output signal 529 that is Q-mode signal 521 whenever Q-mode enable 527 is 1; the output signal 529 is the data mode signal 523 whenever Q-mode enable 527 is "0." Subsequent processing stages in the ADSL transmitter convert the output signal 529 into a signal that is transmitted by the ADSL transmitter.

[0039] Fig. 6 is a flow diagram of overall control for mode selection in accordance with the present invention. First, inputs to the system are examined (block 601). "Inputs" may be, for example, user data, internally generated overhead data (e.g., system status or commands), etc., or no data at all. If it is determined that data is present at the inputs (block 603), then a determination is made whether the system is in the data mode (block 605). If the system is indeed in the data mode, the system simply operates in the data mode (block 607). If it is not in the data mode (as determined at block 605), the system first configures the scrambler for data mode operation (block 609), and then operates in the data mode (block 607).

[0040] If, on the other hand, it is determined that no data is present at the inputs (block 603), then a determination is made whether the system is in Q-mode (block 611). If the system is indeed in Q-mode, the system simply operates in Q-mode (block 613). If it is not in Q-mode (as determined at block 611), the system first configures the scrambler for Q-mode operation (block 615), and then operates in Q-mode (block 613).

[0041] Fig. 7 is a depiction of a generic scrambler that may be employed in connection with the present invention. Scrambler 701 outputs a pseudo random bit sequence with a period of 2^N-1, where each of $j_1 j_2 ... j_N$ comprises one of "0" or "1" and $\{j_1 j_2 ... j_N\}$ (not all equal to "1") represents the initial state of the scrambler 701. $\{c_1, c_2 ... c_N\}$ represents the coefficients of a primitive polynomial.

[0042] Fig. 8 is one specific embodiment of the scrambler of Fig. 7 that may be employed in connection with the present invention. Scrambler 801 is defined for ADSL data transmission in G.992.1 and G.992.2. The scrambler 801 of Fig. 8 is based on the primitive polynomial $1 \oplus x^{18} \oplus x^{23}$ with the $\oplus$ symbol used to denote addition mod 2. When the scrambler 801 input is clamped to "1," the scrambler 801 output becomes a pseudo-random bit sequence with a period of 2^{23}-1.

[0043] To consider the randomness qualities of the scrambler of Fig. 8, let the sequence $\{a_j, a_{j+1}, a_{j+2}, ...\}$ represent the output sequence emitted by the scrambler with its input clamped to one where j is an arbitrary integer representing time. Assume further that the initial state of the scrambler is $\{a_{j+1}, a_{j+2}, ..., a_{j+23}\}$ for some j. Then subsequent outputs of the scrambler are defined by the above primitive polynomial to be

$$a_i = 1 \oplus a_{i-18} \oplus a_{i-23} \text{ for all integer values of } i. \quad (1)$$

Equivalently,

$$a_i \oplus a_{i-18} \oplus a_{i-23} = 1, \quad (2)$$

it being understood that binary arithmetic is being used.

Equation (2) expresses the fundamental recurrence relation for the scrambler of Fig. 8. Further properties of this scrambler make it attractive for generating pseudo-random sequences. Of course, a whole family of scramblers can be defined in a similar way.

[0044] Consider the structure of scrambler 901 of Fig. 9, which is based on the scrambler of Fig. 8 but with alternate outputs selected in such a way that two separate output streams are produced. To determine the randomness properties of the resulting subsequences, let $\{b_i\}$ represent the output sequence obtained by selecting the even-numbered outputs of the master scrambler. That is, let

$$b_i = a_{2i} \text{ for all } i. \tag{3}$$

It is asserted that the $\{b_i\}$ sequence defined by (3) also satisfies Equation (2), which means that $\{b_i\}$ is also a PRBS sequence with all the properties possessed by the $\{a_i\}$ sequence. That is, it is asserted that

$$b_i \oplus b_{i-18} \oplus b_{i-23} = 1. \tag{4}$$

Substituting (3) into (4), the assertion is that

$$a_{2i} \oplus a_{2i-36} \oplus a_{2i-46} = 1. \tag{5}$$

To prove this assertion, note that from (1) we know that

$$a_{2i} = 1 \oplus a_{2i-18} \oplus a_{2i-23}, \tag{6}$$

$$\begin{aligned} a_{2i-18} &= 1 \oplus a_{(2i-18)-18} \oplus a_{(2i-18)-23} \\ &= 1 \oplus a_{2i-36} \oplus a_{2i-41} \end{aligned}$$

from which

$$a_{2i-36} = 1 \oplus a_{2i-18} \oplus a_{2i-41}. \tag{7}$$

Also from (1),

$$\begin{aligned} a_{2i-23} &= 1 \oplus a_{(2i-23)-18} \oplus a_{(2i-23)-23} \\ &= 1 \oplus a_{2i-41} \oplus a_{2i-46} \end{aligned}$$

from which

$$a_{2i-46} = 1 \oplus a_{2i-23} \oplus a_{2i-41}. \tag{8}$$

Substituting (7) and (8) into the left-hand side of (5) we have

$$a_{2i} \oplus 1 \oplus a_{2i-18} \oplus a_{2i-41} \oplus 1 \oplus a_{2i-23} \oplus a_{2i-41} = a_{2i} \oplus a_{2i-18} \oplus a_{2i-23} \quad (9)$$

$$= 1 \quad (10)$$

from (2) with i replaced by $2i$. The chain of implications just navigated shows that

$$b_i \oplus b_{i-18} \oplus b_{i-23} = 1 \quad (4)$$

as was asserted. Therefore, the sequence, $\{b_i\}$ obtained by selecting the even-numbered outputs of the master scrambler is, itself, a PRBS sequence with the same randomness properties as that of the master scrambler. A similar argument proves that the sequence obtained by selecting the odd-numbered outputs of the master scrambler also is a PRBS sequence with the same randomness properties as the master scrambler.

[0045] An embodiment with exactly similar properties (except that the bit sequence is inverted) obtains when a PRBS generator is substituted for the scrambler. Fig. 10 is a depiction of a generic PRBS generator that may be employed in connection with the present invention. PRBS generator 1001 outputs a pseudo random bit sequence with a period of 2^N-1, where each of $i_1, i_2, \ldots i_N$ comprises one of "0" or "1" and $\{i_1, i_2, \ldots i_N\}$ (not all equal to "0") represents the initial state of the PRBS generator 1001. $\{c_1, c_2 \ldots c_N\}$ represents the coefficients of a primitive polynomial.

[0046] Fig. 11 is one specific embodiment of the PRBS generator of Fig. 10 in accordance with the present invention. The PRBS generator 1101 of Fig. 11 is based on the same polynomial as that upon which Fig. 8 is based. To consider the randomness qualities of Fig. 11, let the sequence $\{a_j, a_{j+1}, a_{j+2}, \ldots\}$ represent the output sequence emitted by the PRBS where j is an arbitrary integer representing time. Assume further that the initial state of the generator is $\{a_{j+1}, a_{j+2}, \ldots, a_{j+23}\}$ for some j. Then subsequent outputs of the PRBS generator are defined by the above primitive polynomial to be

$$a_i = a_{i-18} \oplus a_{i-23} \text{ for all integer values of } i. \quad (1)$$

Equivalently,

$$a_i \oplus a_{i-18} \oplus a_{i-23} = 0, \quad (2)$$

it being understood that binary arithmetic is being used.

[0047] Equation (2) expresses the fundamental recurrence relation for the PRBS generator. Further properties of this PRBS generator make it attractive for generating pseudo-random sequences. Of course, a whole family of PRBS generators can be defined in a similar way.

[0048] Consider the structure of PRBS generator 1201 of Fig. 12, which is based on the PRBS generator of Fig. 11, but with alternate outputs selected in such a way that two separate output streams are produced (in accordance with the present invention). To consider the randomness qualities of the scrambler 1201 of Fig. 12, let $\{b_i\}$ represent the output sequence obtained by selecting the even-numbered outputs of the master PRBS generator. That is, let

$$b_i = a_{2i} \text{ for all } i. \quad (3)$$

It is asserted that the $\{b_i\}$ sequence defined by (3) also satisfies Equation (2), which means that $\{b_i\}$ is also a PRBS sequence with all the properties possessed by the $\{a_i\}$ sequence. That is, it is asserted that

$$b_i \oplus b_{i-18} \oplus b_{i-23} = 0. \quad (4)$$

Substituting (3) into (4), the assertion is that

$$a_{2l} \oplus a_{2l-36} \oplus a_{2l-46} = 0. \quad (5)$$

To prove this assertion note that from (1) we know that

$$a_{2l} = a_{2l-18} \oplus a_{2l-23}, \quad (6)$$

$$\begin{aligned} a_{2i-18} &= a_{(2i-18)-18} \oplus a_{(2i-18)-23} \\ &= a_{2i-36} \oplus a_{2i-41} \end{aligned}$$

from which

$$a_{2l-36} = a_{2l-18} \oplus a_{2l-41}. \quad (7)$$

Also from (1),

$$\begin{aligned} a_{2i-23} &= a_{(2i-23)-18} \oplus a_{(2i-23)-23} \\ &= a_{2i-41} \oplus a_{2i-46} \end{aligned}$$

from which

$$a_{2l-46} = a_{2l-23} \oplus a_{2l-41}. \quad (8)$$

Substituting (6), (7), and (8) into the left-hand side of (5) we have

$$\begin{aligned} a_{2i} \oplus a_{2i-18} \oplus a_{2i-41} \oplus a_{2i-23} \oplus a_{2i-41} &= a_{2i} \oplus a_{2l-18} \oplus a_{2l-23} \quad (9) \\ &= 0 \quad (10) \end{aligned}$$

from (2) with i replaced by $2i$. The chain of implications just navigated shows that

$$b_l \oplus b_{l-18} \oplus b_{l-23} = 0 \quad (4)$$

as asserted. Therefore, the sequence, $\{b_l\}$, obtained by selecting the even-numbered outputs of the master PRBS generator is, itself, a PRBS sequence with the same randomness properties as that of the master PRBS generator. A similar argument proves that the sequence obtained by selecting the odd-numbered outputs of the master PRBS generator also is a PRBS sequence with the same randomness properties as the master PRBS generator.

[0049] Many modifications and variations of the present invention are possible in light of the above teachings. Thus, it is to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as described hereinabove.

Claims

1. A communication system comprising:

a data communication node; and
a transmitter located in the data communication node, the transmitter having a scrambler, the transmitter using the scrambler to operate in a first, data communication mode and in a second, non-data mode.

2. The data communication system of claim 1 wherein the data communication node comprises an ADSL modem.

3. The data communication system of claim 2 wherein the first, data communication mode comprises SHOWTIME.

4. The data communication system of claim 3 wherein the scrambler scrambles data during SHOWTIME

5. The data communication system of claim 2 wherein the second, non-data mode comprises a Q-mode.

6. The data communication system of claim 5 wherein the scrambler at least partially generates a Q-mode signal.

7. The data communication system of claim 1 wherein the scrambler scrambles data during the first, data communication mode.

8. The data communication system of claim 1 wherein the scrambler at least partially generates a non-data mode signal.

9. A method of operating a transmitter in a data communication system, the transmitter having a scrambler, the method comprising:

determining that data is present at at least one input;
determining whether the scrambler is configured for a data communication mode;
configuring the scrambler for the data communication mode if a determination is made that the scrambler is not configured for the data communication mode;
operating in the data communication mode;
determining that data is not present at the at least one input;
determining whether the scrambler is configured for a non-data mode;
configuring the scrambler for the non-data mode if a determination is made that the scrambler is not configured for the non-data mode; and
operating in the non-data mode.

10. The method of claim 9 wherein operating in the data communication mode comprises scrambling, by the scrambler, data received at the at least one input.

11. The method of claim 9 wherein operating in the non-data communication mode comprises generating, at least partially by the scrambler, a non-data mode signal.

12. The method of claim 9 wherein the transmitter is located in an ADSL modem.

13. The data communication system of claim 12 wherein the data communication mode comprises SHOWTIME.

14. The data communication system of claim 13 wherein operating in the data communication mode comprises scrambling, by the scrambler, data during SHOWTIME

15. The data communication system of claim 12 wherein the non-data mode comprises a Q-mode.

16. The data communication system of claim 15 wherein operating in the non-data mode comprises generating, at least partially by the scrambler, a Q-mode signal.

17. A method of operating a transmitter in a data communication system, the transmitter having a scrambler, the method comprising:

selecting a non-data mode input to the scrambler;
generating, using a first output of the scrambler, a non-data mode signal; and
controlling, using a second output of the scrambler, the output of the non-data mode signal.

18. The method of claim 17 further comprising repeating the generating and controlling for as long as the non-data mode input to the scrambler is selected.

19. The method of claim 17 further comprising:

selecting a data communication mode input to the scrambler; and
scrambling data received for communication.

20. The method of claim 19 wherein the transmitter is located in an ADSL modem.

21. The data communication system of claim 20 wherein the data communication mode comprises SHOWTIME.

22. The data communication system of claim 20 wherein the non-data mode comprises a Q-mode.

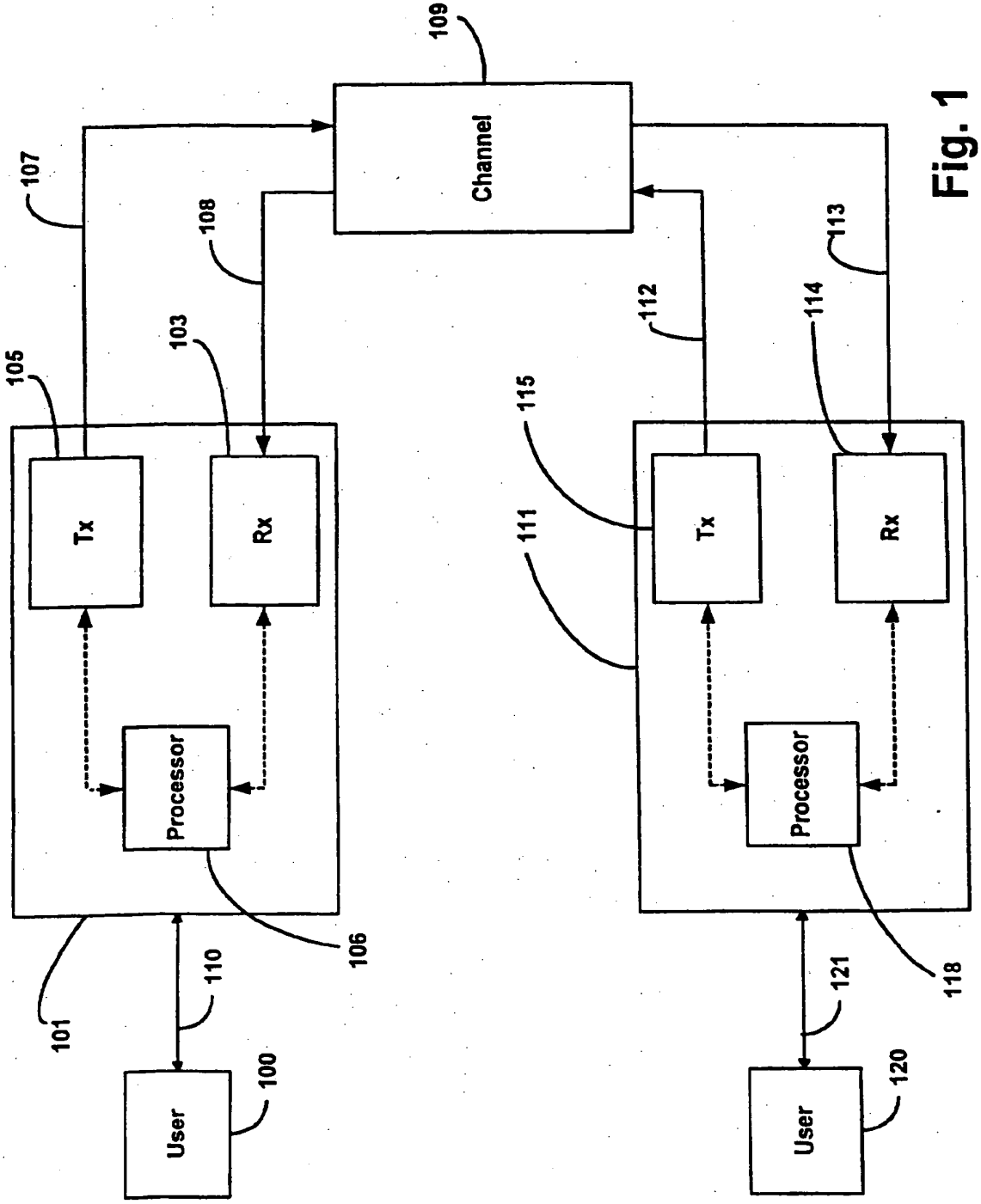
109
Channel
107
108
103
105
112
114
115
111
113
Tx
Rx
Tx
Rx
Processor
Processor
106
101
110
121
118
User
User
100
120

Fig. 1

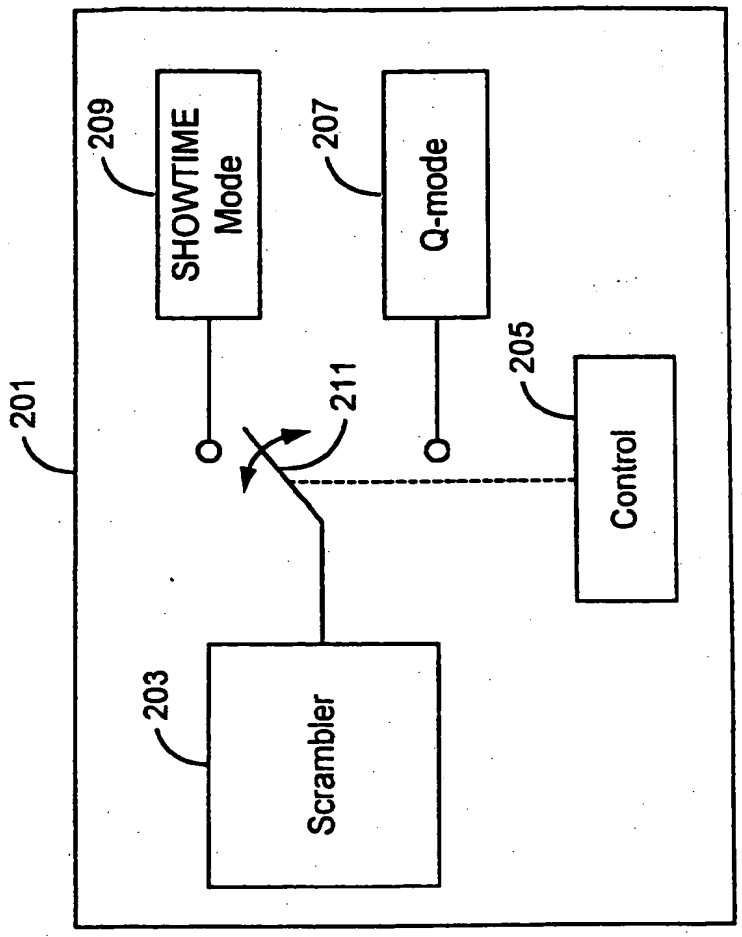
201
209
SHOWTIME Mode
207
Q-mode
205
211
Control
203
Scrambler

Fig. 2

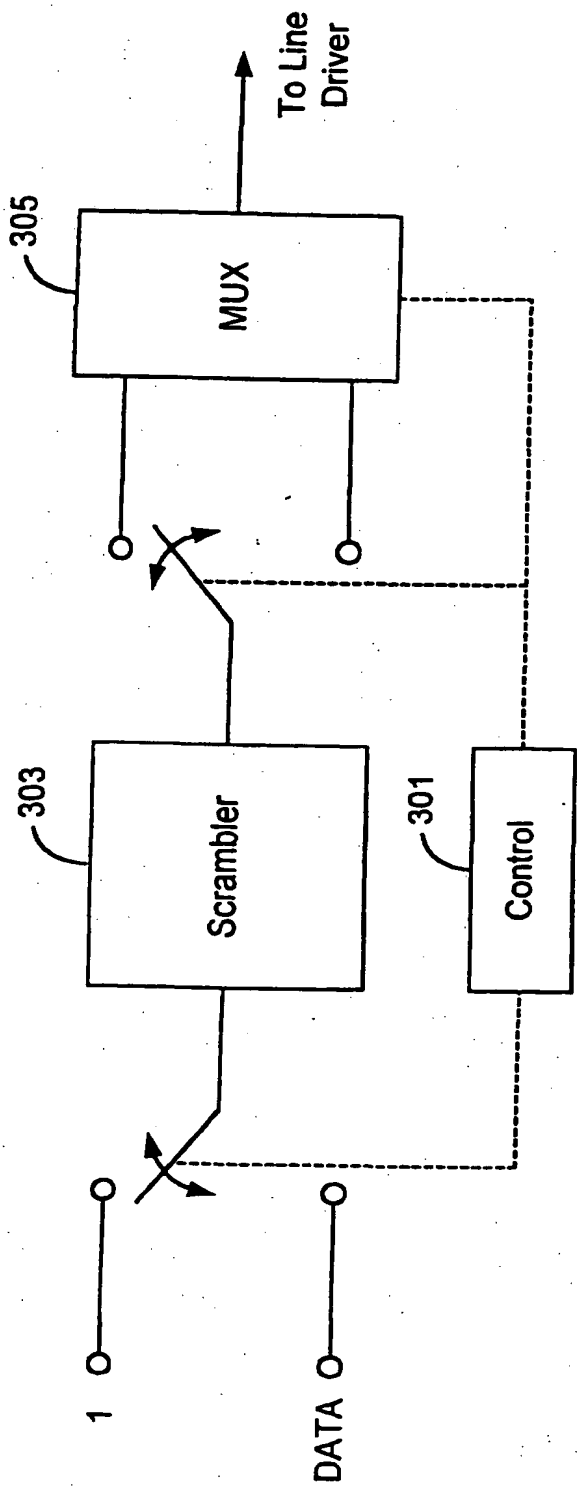

Fig. 3

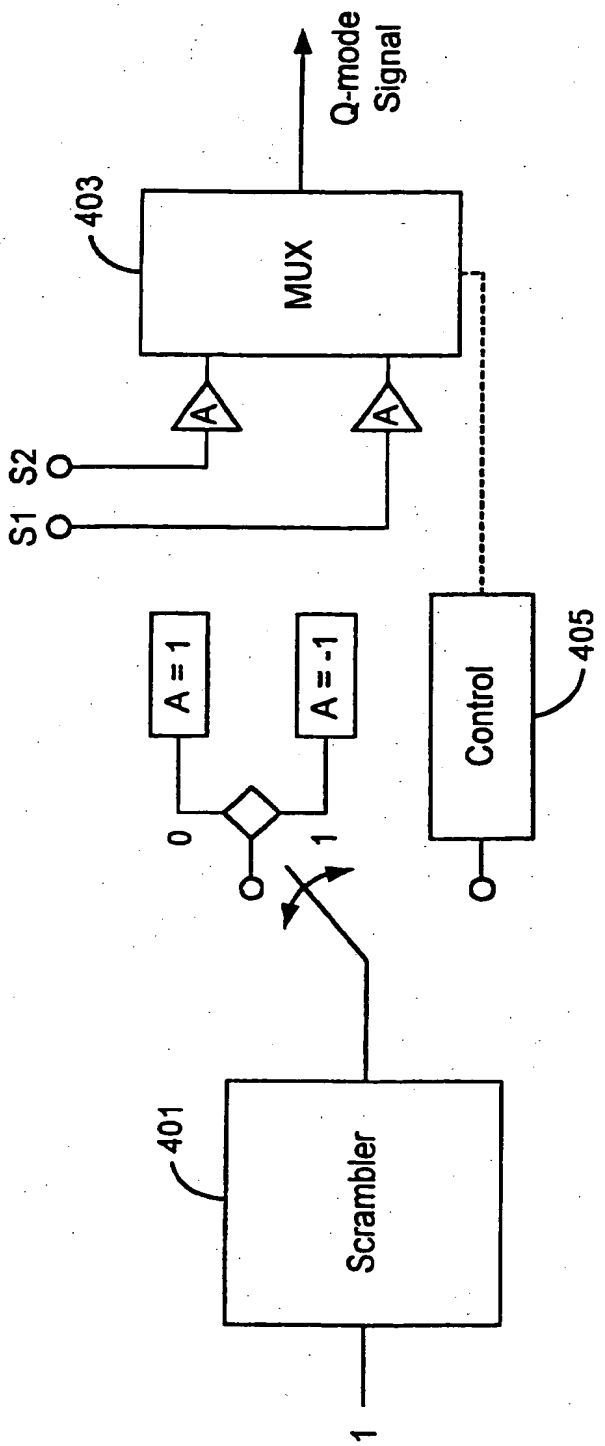
Q-mode Signal
403
MUX
A
A
S2
S1
A = 1
A = -1
Control
405
0
1
401
Scrambler
1

Fig. 4

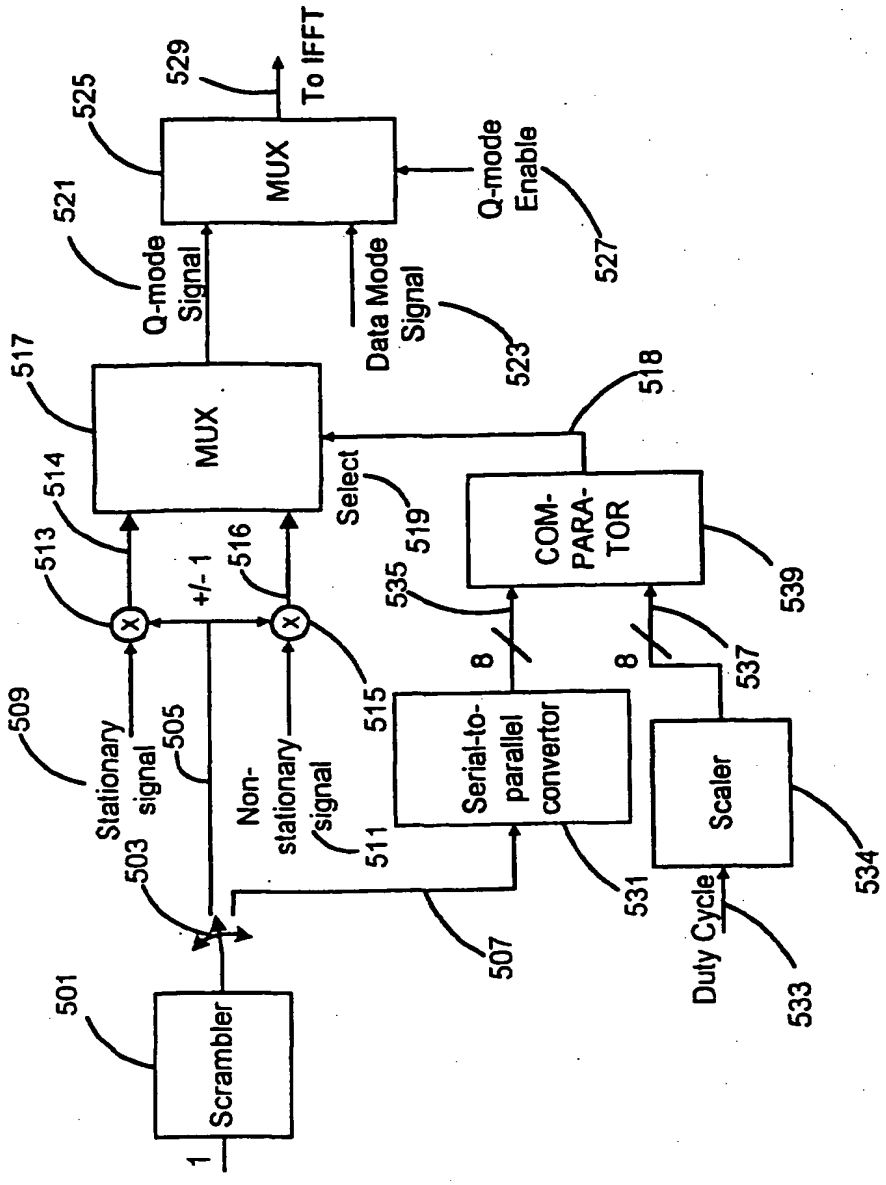
Scrambler
501
1
Stationary signal
509
Non-stationary signal
505
503
507
+/- 1
513
516
515
Serial-to-parallel convertor
511
8
531
Scaler
534
Duty Cycle
533
COM-PARA-TOR
539
535
Select
519
518
MUX
517
514
Q-mode Signal
521
Data Mode Signal
523
MUX
525
Q-mode Enable
527
To IFFT
529
8
537

Fig. 5

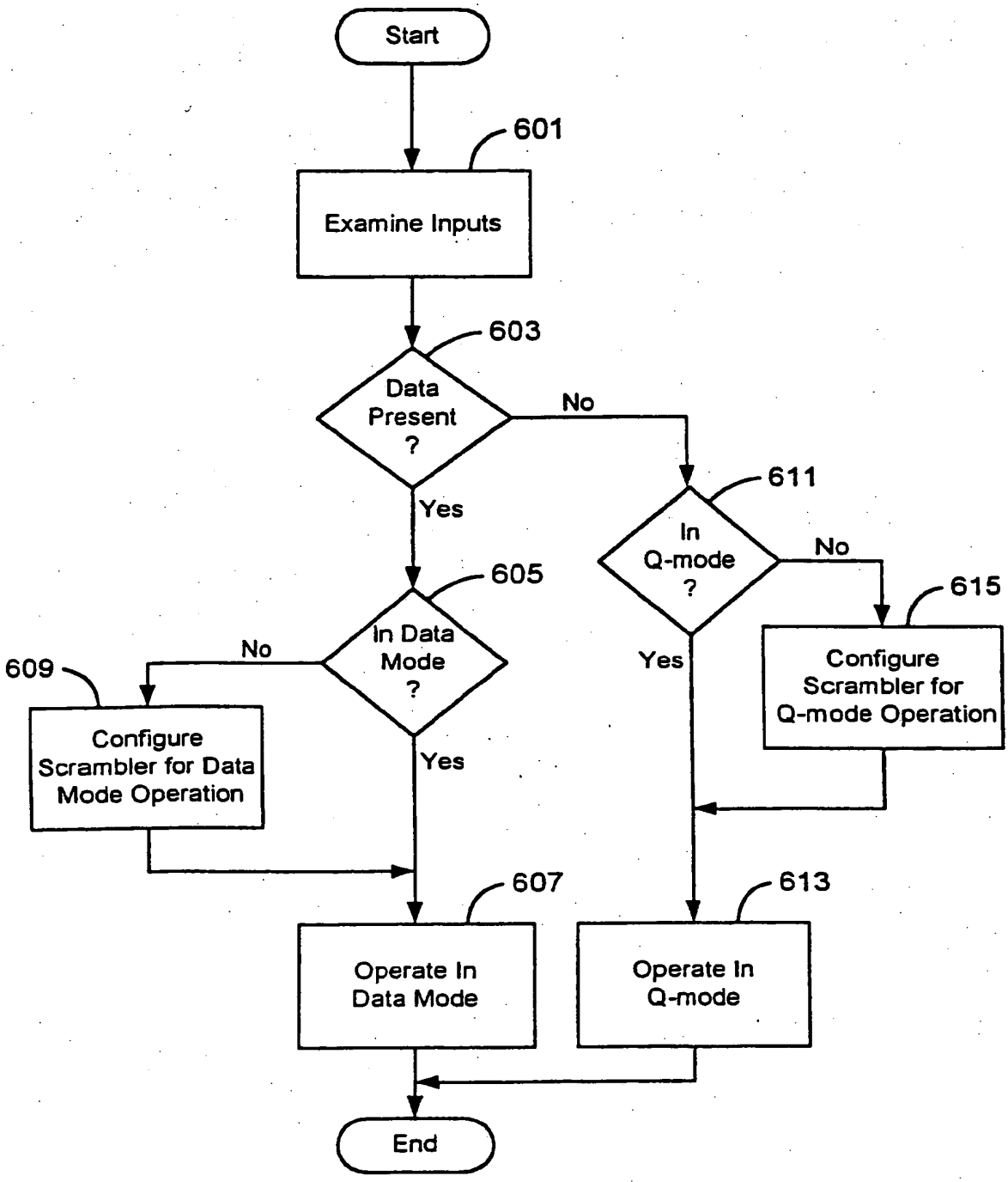
Start
601
Examine Inputs
603
Data Present ?
No
Yes
611
In Q-mode ?
No
615
Configure Scrambler for Q-mode Operation
Yes
605
In Data Mode ?
No
609
Configure Scrambler for Data Mode Operation
Yes
607
Operate In Data Mode
613
Operate In Q-mode
End

Fig. 6

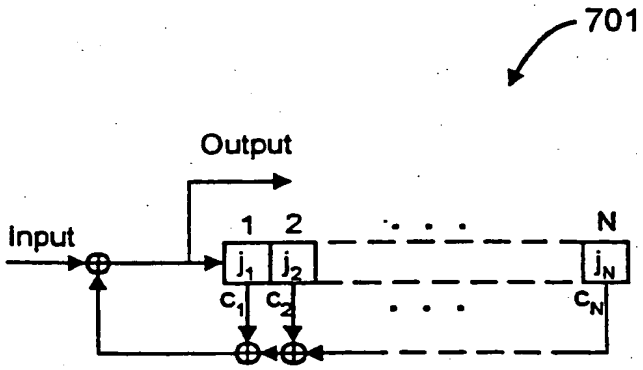

Fig. 7

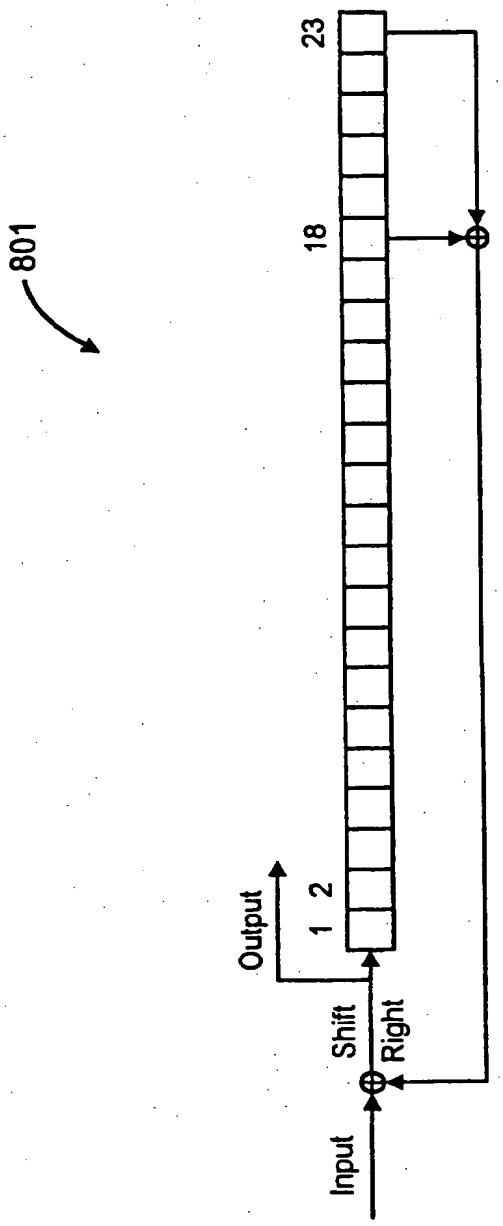

Fig.8

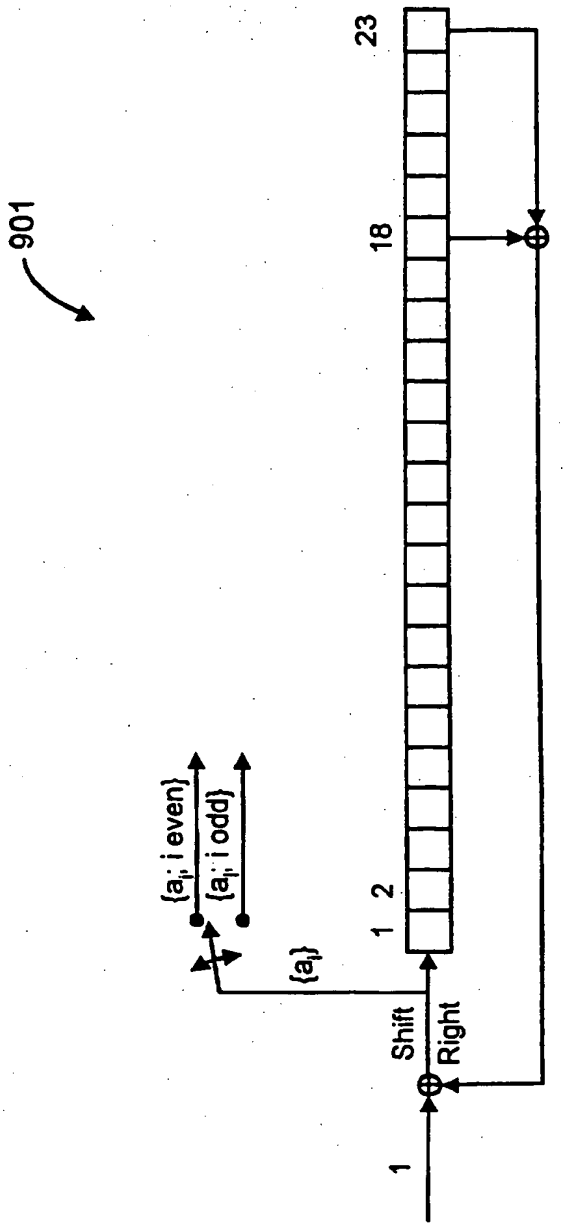

Fig. 9

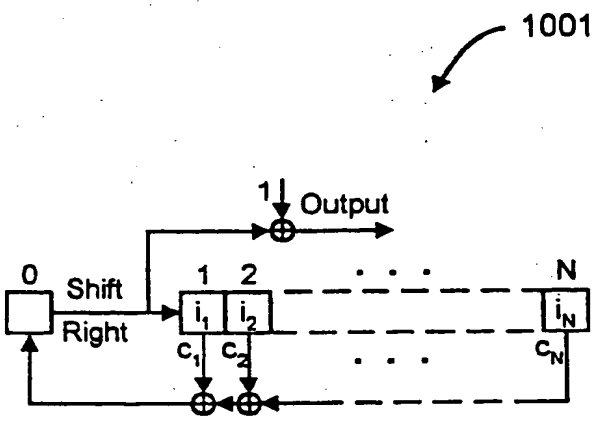

Fig. 10

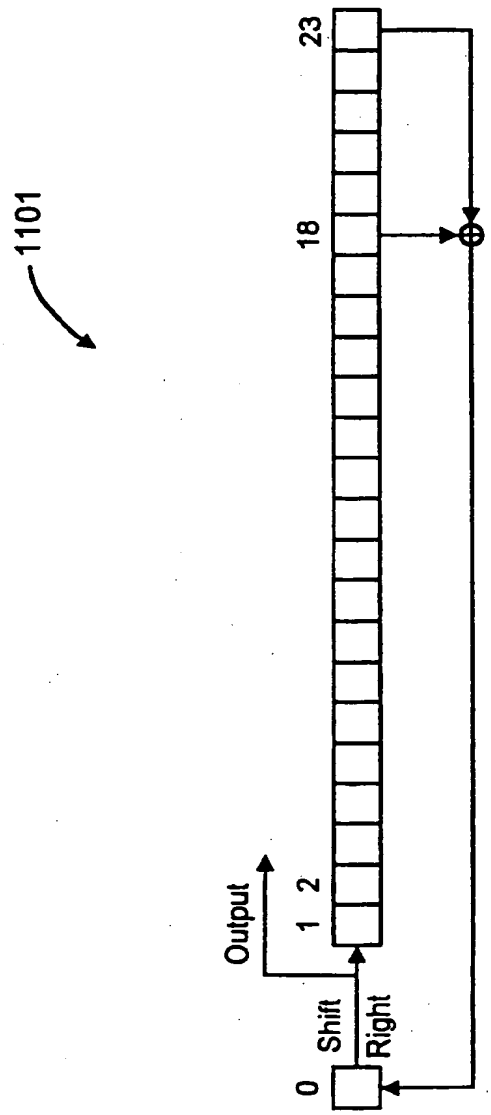

Fig. 11

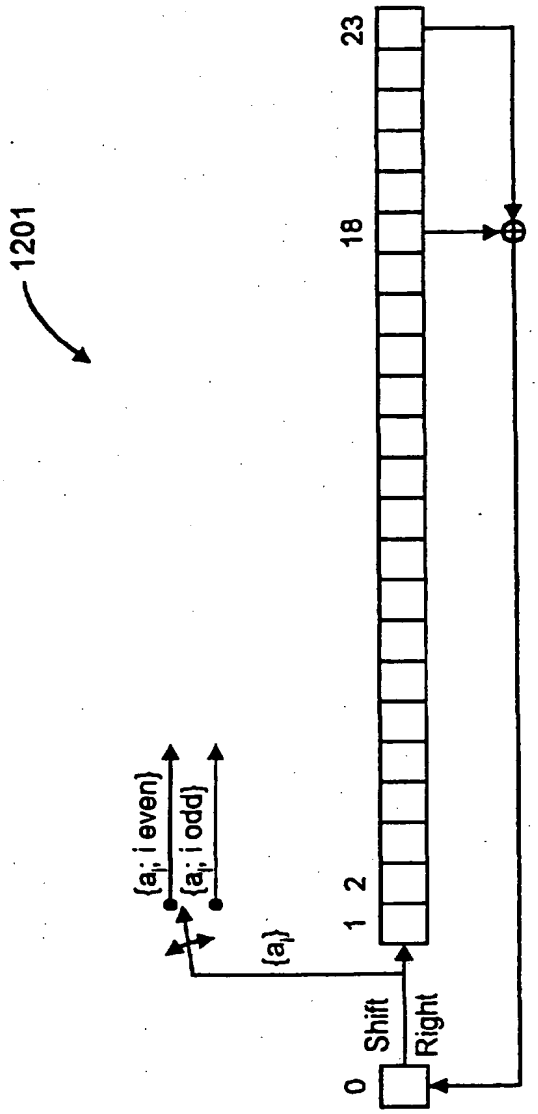

Fig. 12